REMARKS

This amendment responds to the Office Action mailed August 7, 2001. Filed concurrently herewith is a *Request for a Two Month Extension of Time* which extends the shortened statutory period for response to expire on January 7, 2002. Accordingly, applicant respectfully submits that this response is being timely filed.

Claims 1-48 were pending. In this submission, claims 1 and 10 have been amended to more clearly define protection to which Applicants are entitled, and claims 12-48 are canceled without prejudice or disclaimer. Thus, claims 1-11 are now pending in the present application and, for the reasons set forth below, are believed to be in condition for allowance.

The present invention is directed to a processor for executing instructions in units that are unrelated to the units in which the instructions are read from a program. The processor reads instructions from memory according to a first program counter which indicates a storage position of a processing packet in the memory. The processing packet has a size which is an integer number of bytes, and the storage position corresponds to a byte boundary. A second program counter is provided which indicates a position of a processing target instruction within the processing packet read from memory, where the processing target instruction position is not required to correspond to a byte boundary. As a result, the instructions to be executed can be freely set regardless of the amount of data read from memory. This allows instructions whose word length is not an integer number of bytes to be executed even when processing packets are read from memory in units of an integer number of bytes.

FORMALITIES

The Office Action objected to FIGS. 35A and 35B as not containing a clear boundary between the figures. Filed concurrently herewith is a *Request for Drawing Change Approval* which corrects FIGS. 35A and 35B to put proper spacing between the figures. Review and approval of these corrections is respectfully requested.

An IDS was filed on August 10, 1999 submitting Japanese Laid-Open Patent Application No. 62-42237 to the U.S. Patent Office along with a partial English translation of this reference. This reference was not considered by the Examiner, since the form PTO 1449 submitted with the IDS did not indicate that a partial translation was submitted. As requested by the Examiner in the Office Action, filed concurrently herewith is a revised form PTO 1449 which identifies that only a partial translation (Abstract) of the Japanese reference has been submitted. Thus, Applicants respectfully request consideration of this reference.

The Office Action rejected Claims 10-11 under 35 U.S.C. § 112, first paragraph, as containing subject matter not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention. Applicants respectfully traverse this rejection, and reconsideration is requested based on the following remarks.

Claim 10 recites that a processing packet has a length of *n* bytes. It is asserted in the Office Action that *n* is an arbitrary integer which is undetermined, and the Office Action asserts that the specification does not teach how to determine the number *n*. Contrary to this assertion, *n* is in fact a determined number representing the fixed length of the processing packet. The length of the processing packet does not vary, where such processing packets have fixed lengths which do not need to be determined. The Examiner's attention is directed to page 34, lines 8-11 of the present specification which recites: "the processor of the present embodiments reads instructions using **packets of a fixed length**, but only executes a suitable number of

units in each cycle depending on parallelism of the instructions" (emphasis added). The processor reads processing packets having a fixed length, *n*, which will be a function of the processor. As such, the processor does not require logic to detect the integer *n*. Applicants respectfully submit that the subject matter claimed in Claims 10-11 is properly described in the specification in such a way as to enable one skilled in the art to make and/or use the invention, and reconsideration is respectfully requested.

PRIOR ART REJECTIONS

The Official Action rejected Claims 1-11 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,559,975 to *Christie et al.* This rejection is respectfully traversed in view of the above amendments, and reconsideration is requested based on the following remarks.

Independent Claim 1 recites a processor for reading instructions from memory according to a program counter and for executing the read instruction. Instructions are executed in units that are unrelated to the units in which the instructions are read from a program. In order to accomplish this feature, the program counter includes a first program counter which indicates a storage position of a processing packet in the memory. Claim 1 has been amended to recite that the processing packet has a size which is an integer number of bytes, where the storage position is a position corresponding to a byte boundary. The program counter further includes a second program counter which indicates a position of a processing target instruction within the processing packet read from memory, even if the position does not correspond to a byte boundary. Claim 1 has been amended to recite that the position of the processing target instruction is regardless of whether the position corresponds to a byte boundary. This allows instructions whose word length is not an integer number of bytes to be executed even when processing

packets are read from memory in units of an integer number of bytes, and enables the processor to execute instructions which are not byte-aligned.

Christie discloses a program counter update mechanism having a program counter having a 'less significant program counter portion' and a 'more significant program counter portion.' The 'less significant program counter portion' provides "less significant value bits" which indicate a position of a processing target instruction based on a selected one of a plurality of "less significant value bits" that are received, see col. 10, lines 42-65 and col. 18, lines 4-23. The 'more significant program counter portion' includes an incrementor to increment the present program counter value to the next instruction. As discussed in the Office Action, the 'less significant program counter portion' and the 'more significant program counter portion' include adders, multiplexers, and other operators. The 'less significant value bits' are produced by addition or other general binary operation for providing the lower order bits of a memory address. Given the fact that these 'less significant value bits' are produced from these lower order bits, it appears necessary that the memory address must be located on a byte boundary. It does not appear that the program counter of *Christie* is capable of indicating a position of a processing target instruction that is not on a byte boundary. Thus, the program counter of *Christie* does not execute non-byte aligned instructions. As indicated above, independent Claim 1 of the present invention recites that the second program counter indicates a position of the processing target instruction, even if the position does not correspond to a byte boundary. *Christie* does not appear to disclose this feature, and Applicants respectfully submit that *Christie* neither anticipates nor renders obvious Claim 1 and its respective dependent claims 2-11. Reconsideration is respectfully requested.

Applicant respectfully submits that all pending rejections have been overcome and Claims 1-11 are in proper condition for allowance. Early issuance of a Notice of Allowance is earnestly solicited. If a telephone or further personal conference would be helpful, the Examiner is invited to call the undersigned, who will cooperate in any appropriate manner to advance prosecution.

Respectfully Submitted,

PRICE AND GESS

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I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to the Assistant Commissioner for Patents, Washington DC 20231
on 1-7-02
Melissa Sanchez

Signature
1-7-02
Date

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims have been amended as follows:

1. (Amended) A processor for reading instructions from a memory according to a program counter, [the memory storing instructions in one-byte units] and for executing the read instruction,

the program counter including a first program counter and a second program counter,

the first program counter indicating a storage position of a processing packet in the memory, the processing packet [being composed of an integer number of the one-byte units] being made of an integer number of bytes, the storage position being a position corresponding to a byte boundary,

the second program counter indicating a position of processing target instruction in the processing packet regardless of whether the position corresponds to a byte boundary, the processing target instruction being an operation to be executed by the processor.

11. (Amended) The processor of Claim 10, further including

an instruction buffer for temporarily storing instructions; and

instruction reading means for transferring instructions [with a minimum transfer size of one one-byte unit] being made of an integer number of bytes from the memory to the instruction buffer, in accordance with available space in the instruction buffer but regardless of a size of a processing packet.

FORM PTO-1449 (REV. 7-80) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

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APPLICANT: Shuichi Takayama et al.	
FILING DATE: April 28, 1999	GROUP: 2122

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPRO-PRIATE
	A						
	B						
	C						
	D						
	E						
	F						
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	I						
	J						
	K						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANS-LATION YES	TRANS-LATION NO
	L	6 2 4 2 2 3 7	02/24/87	Japan			x Partial	
	M							
	N							
	O							
	P							
	Q							

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

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EXAMINER | DATE CONSIDERED

*EXAMINER: Initial if references considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered.

INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.